The Value of In-line, Product Wafer Metrology for Critical Processes.

The value of in-line, product wafer testing of process results for critical process steps is in two general areas:

1. Timely and comprehensive evaluation of process effects and
2. Reduction of the value of wafers-at-risk following critical steps.

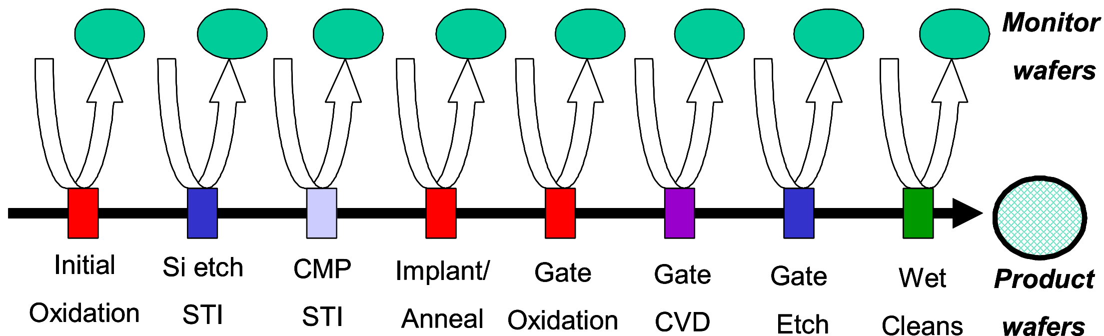
Comprehensive Evaluation of Process Effects

The measurement of properties of device wafer structures following critical process steps, such as dielectric film growth or deposition, has an intrinsic advantage over the use of monitor wafers to track the performance of process equipment in that the product wafer is sensitive to the cumulative effects of the entire process flow, while a monitor wafer samples a segment of the total process environment. For example, the effects of pre-process wafer cleans prior to dielectric film formation and environmental effects (exposure to gases, etc.) during photoresist processing are difficult to include into routine monitor wafer flows.

Product wafer testing has the additional advantage that there are no added costs from monitor wafer use and reduced throughput of critical process tools for monitor processing. These concepts are suggested in Figure 1.

Product wafers **are exposed to the** ***cumulative process flow,*** **including litho, resist cleans, wafer transport and other processing.**

Have Direct Correlation to Yield



Monitor wafers **sample** ***individual process cycles*** **and are inadequate screens for multi-process, correlated effects.**
Monitor wafers also cost extra money and reduce production capacity.

Figure 1. Sketch of comparison of product and monitor wafer flows for metrology on critical process steps.

Reduction of Value of Wafers at Risk

The value of the time delay between completion of a critical process steps and the review of metrology information on the performance of the process can be measured in terms of the value of the total wafer flow through the process step during that interval. The average number of wafers per hour processing a production line can be estimated from the number of wafer starts per month. For example, for a production line with 30,000 wafer starts per month, approximately 1,000 wafers are processed in a 24 hour period; or ~42 wafers/hour. The monetary value of these wafers can be estimated by the usable die per wafer (typically ~200) and t he value of the individual die (a few pennies to several hundred dollars, ~US$2 for a figure of merit estimate, or $500/wafer).

For the case of dielectric film formation, a comparison can be made of the risk of testing the film quality directly or after deposition and patterning of poly-Si capacitor test structures. A process flow outline and estimated minimum wafer flow time for post-dielectric film formation process is shown in Table 1. An estimated minimum process time for a routine flow from dielectric film formation to the start of capacitor testing using poly-Si capacitors is 12 hours. The actual delay will depend on the fab loading and queue procedures at each process step.

Table 1. Estimated minimum process steps and time for formation of poly-Si test capacitor for dielectric film characterization, exclusive of measurement and analysis time.

Process Step	Time (hr)	Cumulative Time (hr)
Dielectric film growth		
EOT measurement		
Doped poly-Si dep	4	4
PR spin	1	5
Litho exposure	1	6
PR develop	1	7
Poly-Si etch	3	10
PR strip	1	11
Residual PR clean	1	12
EOT measurement		

An estimate of the value of wafers at risk, equal to the value of wafers processed during the time interval between a critical processes step and analysis of metrology evaluation of the quality of the materials on the wafer, is shown in Fig. 2 for the case of a nominal wafer value of $500/wafer.

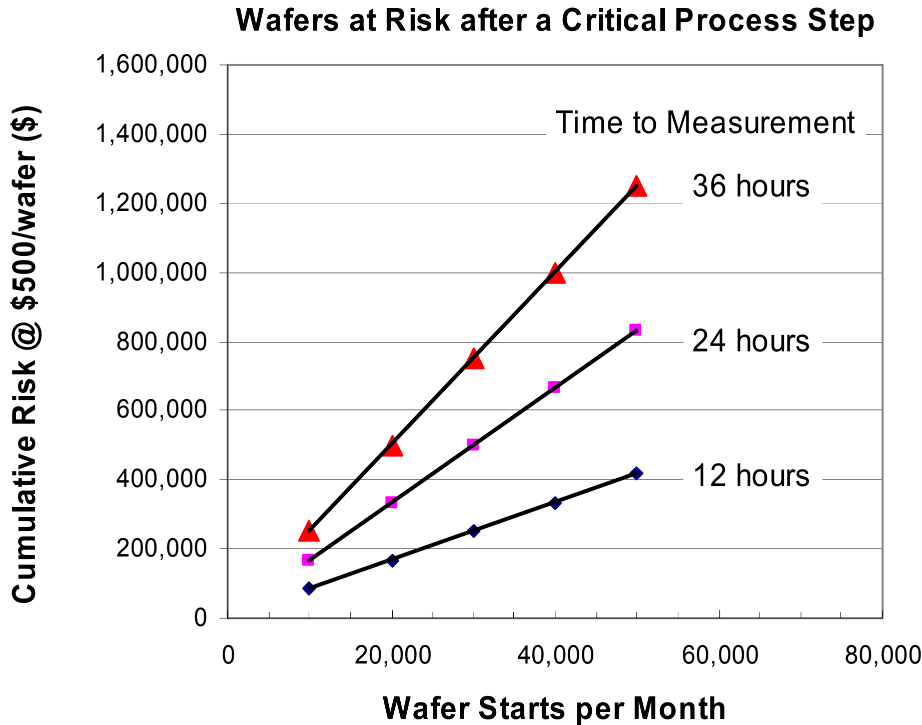


Figure 2. Value of wafers at risk following a critical process step for 12, 24 and 36 hour delays between the process step and completion of testable structures. This does not include the additional time for measurement and critical analysis of the data.

For the example of a 30,000 wafers/month loading and a $500/wafer value, the value of wafers at risk for a 24 delay between dielectric film formation and analysis of testing data is ~$0.5M. This could be taken as a typical risk for routine evaluation for dielectric film properties with a poly-Si capacitor structure.

Evaluation of dielectric film properties (EOT, Vfb, Qit, QBD, etc.) by direct probing of the dielectric film on a product wafer immediately after film formation can reduce the time delay to less than 1 hour, with a corresponding decrease of the value of wafers at risk to <$21k.

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