RsL Applications Note:

Doping Metrology for Ultra-shallow Junctions

Summary

The ITRS05 requirements for high-performance logic transistors call for an immediate ~40 % decrease in desired source/drain extension junction depth in order to maintain CMOS performance advances in the face of expected delays in implementation of metal gates and high-k dielectrics. This places increased pressure on process and metrology for ultra-shallow (<10 nm) junctions (USJ). Applications of non-contact RsL measurements for RTP and laser annealed wafers are discussed along with illustrations of the limitations of contact probes for USJ due to probe penetration and junction leakage.

Activation and leakage challenges for SDE

The ITRS05 transistor roadmap projects the continued lateral and vertical scaling of transistor dimensions, while holding the maximum allowed source/drain extension sheet resistance nearly constant [1]. Source/drain extension (SDE) junction depths in the IRTS05 models are ~40% shallower than the trends that had been used in the 2001 and 2003 ITRS projections (which used Xj (SDE) = $0.55*L_{gate} \pm 25\%$) (Fig.1). The new Xj values are based on full transistor modeling, taking into account the effects of dielectric thickness scaling and poly-Si gate depletion. With the ongoing delays in the availability of high-k dielectrics and suitable processes for integration of multi-work function metal gates, the continued requirements for increased transistor performance push the need to scale the SDE Xj to ~$0.35*L_{gate}$.

To achieve these increasingly shallow junctions with increasing dopant activation levels, new process technologies for both implantation and annealing are needed. Low energy implantation by single ions in beam line implanters will compete with new technologies for implantation, such as molecular and cluster ion beams containing large numbers (10 to >2,000) of atoms as well as new forms of plasma immersion systems. New forms of annealing systems are needed to be implemented in order to limit the time at high (>1100 C) temperatures to the order of ms by using either flash lamps or scanned laser beams.

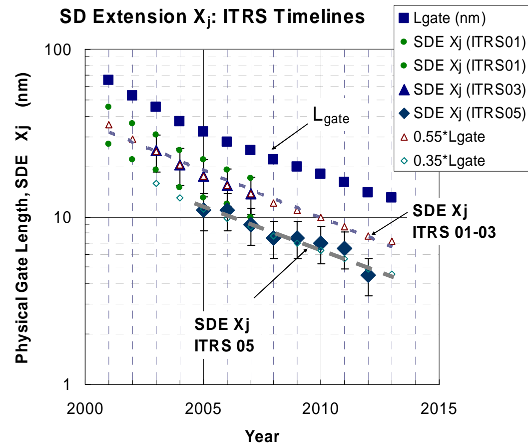


Figure1. Source/drain extension (SDE) junction depths (Xj) and gate lengths for ITRS 01, 03 and 05. For ITRS01-03 the SDE Xj was modeled as $0.55*L_{gate} \pm 25\%$. The ITRS05 projections are close to Xj (SDE) = $0.35*L_{gate} \pm 25\%$.

Non-contact method for sheet resistance and leakage current metrology: RsL

The Frontier Semiconductor con-contact sheet resistance, Rs, and leakage current, RsL, measurement system uses four fundamental processes to obtain measurements of p-n junction electrical characteristics. First, a modulated visible light beam illuminates the surface junction and creates electron-hole pairs if the photon energy of the light is greater than the band gap of the semiconductor (1.12 eV for Si, 0.67 eV for Ge, 1.42 eV for GaAs). This internal photo-electron effect creates free carriers which separate according to their charge in the differing chemical potentials of the p-n junction and substrate. Next, the free carriers move out of the region under the light beam by diffusion and drift governed by the sheet resistance of the junction. When the sheet resistance of the junction is low, the spreading of the free carriers extends over larger distances than for higher resistance junctions. The spatial extent of the carrier spreading is sensed by a pair of AC-coupled electrodes a small (~1 mm) distance above the p-n junction. One electrode is directly over the area illuminated by the light beam and one is a short distance away out of the carrier source region (Fig. 2) [2].

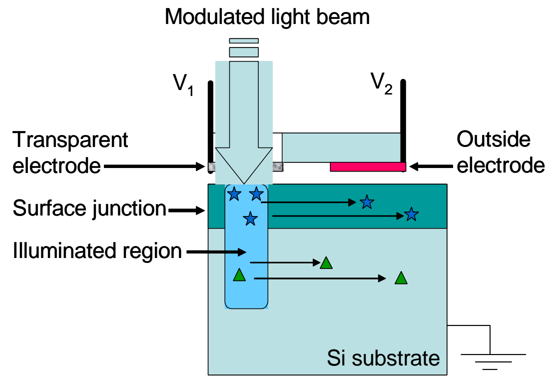


Figure 2. Non-contact probe of p-n junction sheet resistance and leakage current.

The ratio of the junction photo-voltage (JPV) signals collected in the two electrodes, V_1/V_2, is determined by the junction sheet resistance, Rs, leakage current, Io, and capacitance, Cs, which are separately determined in the RsL method. Measured ranges for Rs is from 10 to >300,000 Ohm/square, for leakage current from 10^{-7} to $>10^{-2}$ A/cm^2 and the junction capacitance has been determined for substrate doping ranging from $2x10^{14}$ to $>10^{19}$ dopants/cm^3. The measurements are remarkably stable, with standard deviations for repeated measurements for Rs at <0.1 % for Rs in the range from 100 to 300,000 Ohm/square for junction depths from <10 nm to >2 um.

RsL Characterization of RTP Anneals

Rapid Thermal Processing (RTP) anneals have been the mainstay of contemporary thermal annealing with dopant activation anneals at ~1050 C for 1 to 5 s. To achieve uniform thermal cycles across a 200 or 300 mm wafer, both the heating and cooling cycles of RTP tool need to be monitored and controlled. For processes which results in relatively deep, ~50 nm and deeper, junctions, RsL measurements of the Rs shift with RTP peak temperature track well with older metrologies, such as 4-point probes (Fig. 3).

The advantage of RsL measurements is that they can be directly extended to shallower junctions, where probe penetration and leakage current effects lead to large errors with 4PP tools. In this way the process control databases can be extended to shorter and hotter anneal cycles in a continuous fashion.

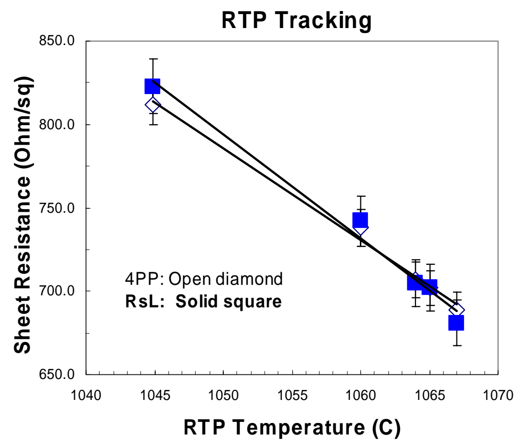


Figure 3. Tracking of sheet resistance with peak RTP temperatures in close agreement with 4PP (for deep, >50 nm, junctions).

The uniformity of RTP anneals can be compromised by a wide variety of effects. The ability of the RsL technique to obtain high-resolution (~10^3 points/wafer) Rs maps, independent of junction leakage current effects, for ultra-shallow junctions (Xj <30 nm) is a key advantage over contact probe methods. In the example shown in Fig. 4, the array of RTP lamps heating the wafer was not balanced properly, resulting in a "hot" region in the center of the wafer (low Rs) and "cooler" heating near the wafer edges, which cool faster than the wafer center due to geometrical effects on radiation cooling. The array of lamps was controlled in circular rings and the wafer was rotating during the anneal, resulting in the strong circular patterns for local variations in Rs visible in the wafer map and the diameter scan.

The cooler thermal history in the outer parts of the wafer, resulting in low activation of the dopants (higher Rs values) also gave poorer annealing of the implant damage, resulting in higher junction leakage currents in the outer regions on the wafer compared to the center. This effect was seen in all RTP annealed wafers in this test, where the wafer centers had low leakage currents and Rs values in the range of 1 to 2 k-Ohm/square and higher Rs values at a radial position of 120 mm and correspondingly higher local leakage currents (Fig. 5).

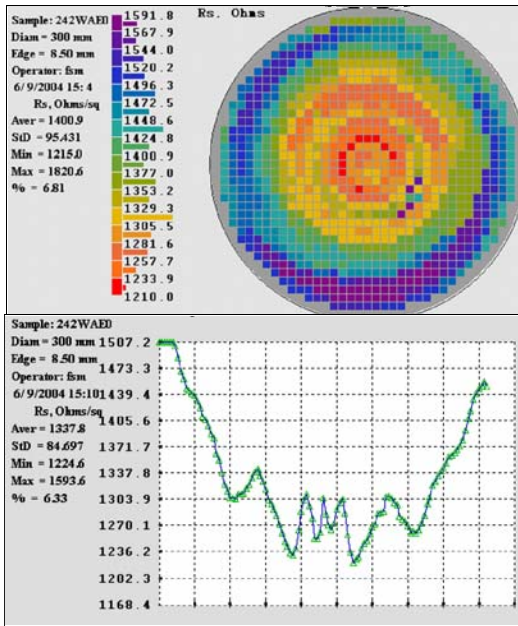


Figure 4. 973 point sheet resistance map (upper) and 121 point horizontal diameter scan (lower) for an RTP annealed wafer with junction depths ~20 nm. The strong circular variations in Rs arise from imbalances in the power levels in ring-shaped arrays of heater lamps and wafer rotation during annealing.

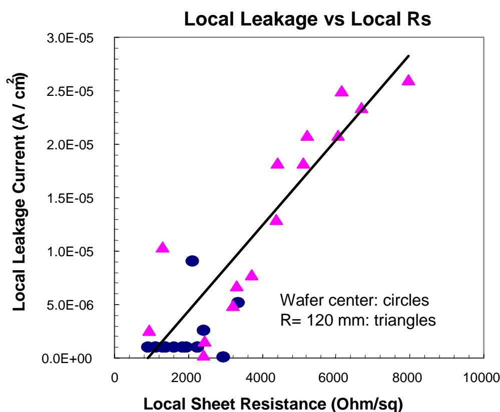


Figure 5. Local Rs and leakage current at wafer centers and at radial position of 120 mm for RTP annealed wafers in the same set an the one shown in Fig. 4.

Wafer holding fixtures can contribute to local heating non-uniformities. In addition to the overall radial variation in dopant activation (cool center, hotter edges, in this case), contact of the wafer to the triangular quartz support pins resulted in a local "hot" spots (lower Rs), perhaps due to local focusing of the RTP lamp intensity (Fig. 6). These local effects are visible in a the 973-point RsL maps and would not be detected with the lower density of probe sites (~120 points/wafer) commonly used with contact probes.

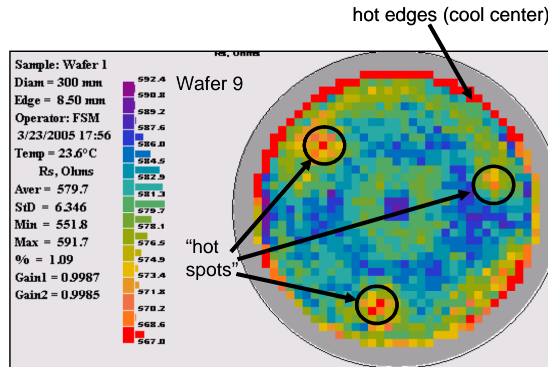


Figure 6. 973-point Rs map of an RTP annealed wafer supported by a triangle of quartz pins, which resulted in local "hot" regions

RsL Characterization of ms-Anneals (Flash lamps and lasers)

As thermal cycle times decrease to the ms-regime in order to suppress dopant diffusion beyond the as-implanted depth, junction metrology is complicated not only by the extreme thinness (~10 nm) of the shallow junction layers but also by the high leakage currents in these junctions arising from the combination of the thin junctions, incomplete dopant activation and high residual levels of lattice damage due to incomplete annealing.

In the case of laser annealing, the challenges of controlling the short, 1 to 10 ms, thermal pulse to high temperatures, 1200 to >1350 C, is complicated by the limited spatial extent of the scanned laser beam, ~1 cm. The annealing process first needs to achieve a net uniform thermal exposure over the entire wafer, including proper overlapping of scanned beams. Characterization of the laser anneal processes requires accurate measurements of ultra-shallow junction sheet resistance and leakage and sufficient spatial resolution to characterize the uniformity of the thermal exposure on the scan of the overlapping laser beams. Preliminary characterization of laser anneal process includes evaluation of the dopant activation uniformity with various beam sizes and scanned overlaps (Fig. 7).

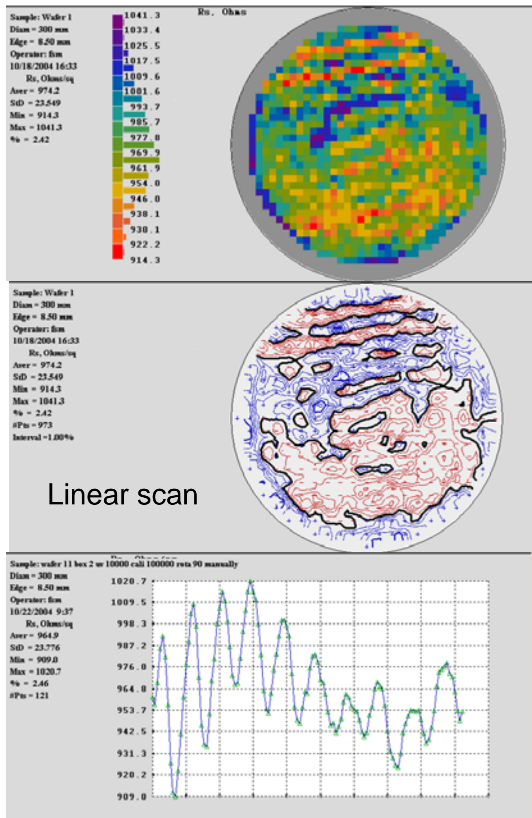


Figure 7. 973-point color and contour maps and a vertical (top to bottom) 121-point diameter scan of sheet resistance for a laser annealed wafer with narrower laser beam size scanned over the upper portion of the wafer.

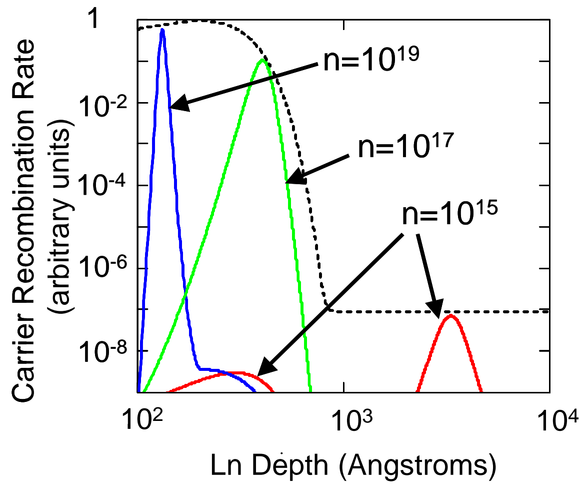
SDE/Halo doping and damage effects on leakage current

Minimizing junction leakage current is a major goal in process optimization of shallow junction technologies. The challenge of leakage current control is strongly increased by the need to form Source/Drain Extension (SDE) junctions in heavily-doped local region ("halos" or "pockets") in order to control short-channel effects in CMOS transistors. The effect of halo doping process in SDE leakage currents is two-fold. First, the high doping levels of a halo region (~10^{19} dopants/cm^3) leads to the formation of a relatively thin depletion or space-charge layer, ~20 nm or less. Since carrier recombination mainly occurs in the central region of the depletion layer, a thinner depletion layer results in increased leakage current, even in the absence of lattice damage, due to the shorter diffusion distances that carriers must traverse before recombination, compared to the conditions in typical test wafers (for 10 Ohm-cm wafers with doping levels at ~ 10^{15} dopants/cm^3, the depletion layer thickness is ~1,000 nm). If, in addition to higher doping levels, there is a large population of lattice defects in the halo region due to incompletely annealed damage from halo, pre-amorphization and SDE doping implants, the large number of recombination centers associated with lattice defects also increases the recombination leakage current levels.

These effects are illustrated in Fig.8 for a calculation of the depth dependence of recombination rates in a depletion layer and the net leakage currents for a 10 nm SDE junction with halo doping and damage profiles centered 20 nm below the SDE junction [3]. For lightly-doped (~10^{15} dopants/cm^3) wafers, the main recombination peak is ~500 nm below the SDE junction and nearby damage, so the net leakage currents are low and not changed when the density of near-surface damage increases. For halo doping at ~10^{19} dopants/cm^3, the recombination peak is close to the SDE junction and is strongly increased by the near-surface damage sites. The effect on leakage current is a strong increase for heavily-doped halo regions and strong sensitivity to lattice defect densities. These model calculations illustrate the promise for reducing junction leakage currents for heavily-doped SDE/halo junctions by managing the creation and annealing of lattice damage levels by innovative approaches to doping and thermal processes.

Contact probe issues: penetration, junction breakdown, leakage

All of these process and technology changes present challenges and opportunities for metrology tools. The combination of shallow junctions and incomplete damage annealing and dopant activation severely limits the viability of contact resistivity probes and increases the importance of accurate measurements of junction leakage currents. For "hard" 4PPs, with probe tips made of WC and similar materials, the first problem is how to achieve good contact with the junction surface without penetrating through the thin junction [4].



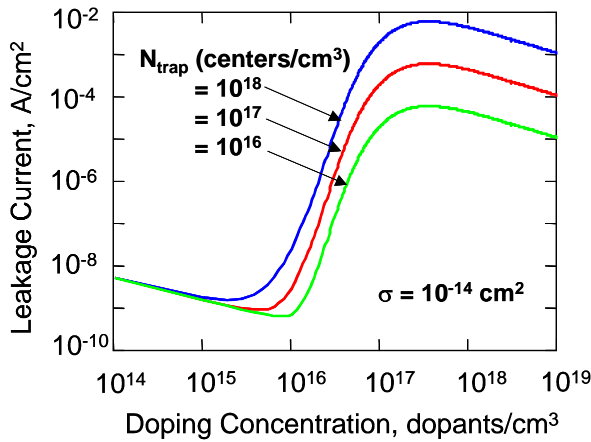


Figure 8. Carrier recombination profiles (top) and corresponding leakage currents (bottom) for SDE/halo junctions with a damage peak 20 nm below the SDE junction [3].

Since the local pressure exerted by 4PP tips typically exceeds the fracture strength of Si, hard probe contacts create "footprints" of crushed Si which are often far deeper than the 20 nm or less doped layer [4]. For these conditions, the probe current also flows into the substrate region of the wafer as well as the surface junction. The parallel current paths into the substrate result in a lower measured sheet resistance when there is probe penetration or substantial leakage current exists (Fig. 9).

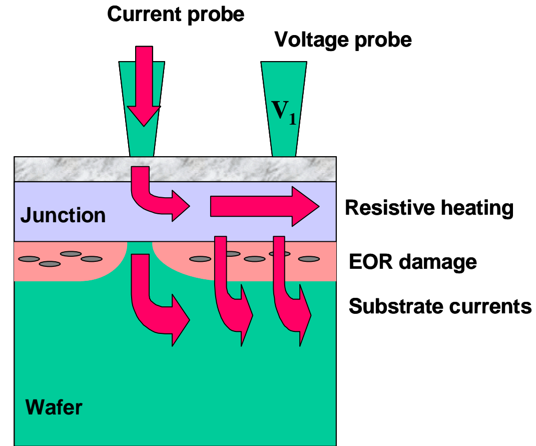


Figure 9. Sketch of 2 probes of a 4-point probe sheet resistance measurement illustrating the possible measurement errors; higher Rs values due to probe current heating of high-Rs layers and lower Rs values due to parallel current flows through the junction and into the wafer (substrate) due to electrical punch-through of the depletion layer under the current injection probe and leakage currents associated with end-of-range (EOR) damage due to incomplete annealing of implant defects. In addition, probe tips can penetrate through the junction region (not shown).

Examples of strong probe punch through effects are shown in Fig. 10 for shallow p^+ junctions implanted into a heavily-doped (~$2x10^{18}$ dopants/cm^3) n-Si wafer. Even for the relatively deep (~35 nm) junctions, the 4PP measurements are ~100x less than the RsL measurements due to errors of additional current flow into the heavily doped wafer. For the shallower junctions, which also had high (10^{-5} to 10^{-3} A/cm^2) leakage currents, the measured sheet resistance is close to the substrate wafer conditions, indicating that almost all of the probe current is flowing through the wafer not the surface junction.

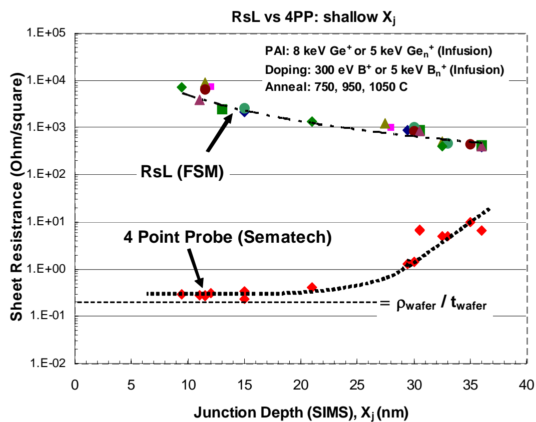


Figure 10. Sheet resistance measurements with RsL (upper curve) and a WC-tipped 4PP (lower curve) for shallow p+-doped junctions in heavily doped n-Si wafers. The 4PP data is consistent with nearly complete breakdown of the surface junction and probe current flow through the n-Si wafer, ~10,000x lower than the RsL measurements for the shallowest (~10 nm) junctions.

Even for non-penetrating 4PP, those using Hg or "elastic metal" tips, measured sheet resistance can still be compromised by electrical punch-through at the current probes and high junction leakage currents. The effect of substrate current flows in contact probes, including test structures, is shown in Fig. 11, where the measured values for non-penetrating 4PPs and a Hall current test structure are compared to RsL values for sheet resistance and leakage current. For junction leakage currents larger than 10^{-4} A/cm^2, the contact probes (either 4PP or Hall current test structure) measured values of sheet resistance decreases relative to the RsL values, going below 10% of the RsL value for leakage currents in the range of 10^{-3} A/cm^2 (for heavily doped, ~10^{18} dopants/cm^3, substrates).

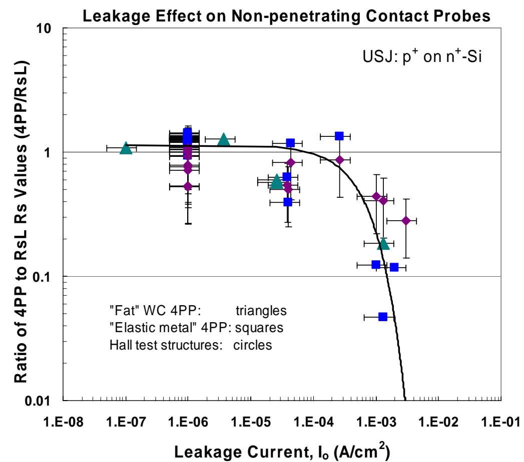


Figure 11. Ratio of contact probe measurements of sheet resistance to RsL values for a large area WC 4PP probe (triangles), an "elastic metal" 4PP (squares) and Hall current test structures (circles) as a function of RsL measurements of leakage current. The confidence levels on the leakage current values is ±50 %, as is the confidence levels for the Rs values from the Hall test structures.

References:

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